REMARKS

Claims 1-21 are pending in the present application. The Examiner has rejected claims 1-21.

I. OBJECTION WITH RESPECT TO THE DRAWINGS

The Examiner has objected to the set of drawings filed on October 27, 2000 as indicated in the Office Action Summary. Applicants assume that the Examiner is requesting a set of formal drawings, although the Office Action is silent as to this point. Therefore, Applicants respectfully submit a formal set of drawings. It is therefore respectfully requested that the objection be withdrawn with respect to the drawings.

II. REJECTION UNDER 35 U.S.C. § 103(a) WITH RESPECT TO CLAIMS 1-22 AND 33-36

Claims 1-21 stand rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,686,867 ("Sutardja") in view of the combination of U.S. Patent No. 5,890,051 ("Schlang") and U.S. Patent No. 5,341,110 ("Nardi"). Applicants respectfully traverse the rejection.

In the Office Action, with respect to each pending independent claim (i.e., claims 1, 8 and 15), the Examiner states that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Nardi to the system of Schlang and Sutardja in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits." Applicants respectfully disagree. For example, Schlang and Nardi cannot be properly combined. Schlang teaches a mobile phone transceiver architecture. On the other hand, Nardi teaches a yttrium-iron-garnet-based (YIG-based) phase-locking oscillator circuit.

YIG resonators require a significant amount of power, generate excessive heat that may harm other transceiver components and require an environment that is free from vibration and electromagnetic interference (EMI). The mobile phones taught by Schlang cannot accommodate a YIG resonator. In particular, mobile phones are sensitive to components consuming significant amounts of power and generating an excessive amount of heat. Furthermore, YIG resonators can be easily destabilized by the movements which are common place with respect to a *mobile* phone as well as movements caused by the environment (e.g., wind). Furthermore, once the YIG-based

phase-locking oscillator circuit is destabilized, it is slow to react and to re-establish phase lock. Support for these and other assertions can be found in the enclosed article, which is not prior art, entitled "Design A Low-Noise Synthesizer Using YRO Technology" by Eliot Fenton et al. Furthermore, the YIG-based phase-locking oscillator circuit taught by Nardi would suffer from the EMI as set forth in Schlang caused by the radio frequency signals distributed along traces on the printed circuit board. See, e.g., Schlang at col. 7, lines 23-31 and lines 62-65. It is well known that YIG resonators operate in a constant magnetic field whose strength determines the frequency of the YIG resonators. A mobile phone with its varying radio frequency signals resonating on the traces of the printed circuit board and on its antenna would generate significant EMI that would destabilize the YIG resonator. Accordingly, Schlang and Nardi teach away from each other and thus teach away from their combination.

In fact, the combination of Schlang and Nardi would render Nardi unsatisfactory for its intended purpose as a low noise reference oscillator. Furthermore, the combination of Schlang and Nardi would render Schlang unsatisfactory for its intended purpose as a mobile phone since the Nardi oscillator circuit would be inoperable in such an environment. Thus, according to M.P.E.P. § 2143.01, there is no motivation or suggestion for combining the teachings of Schlang and Nardi. See, e.g., the section entitled "The Proposed Modification Cannot Render the Prior Art Unsatisfactory for Its Intended Purpose" of M.P.E.P. § 2143.01.

Since the combination of Schlang and Nardi cannot be maintained for at least the above-recited reasons, the Examiner cannot maintain a rejection based upon Sutardja in view of the combination of Schlang and Nardi. It is therefore respectfully requested that the rejection under 35 U.S.C. § 103(a) be withdrawn with respect to claims 1-21.

III. PRIMA FACIE OBVIOUSNESS

Applicants respectfully request that the next Office Action, if necessary, more clearly demonstrate a *prima facie* case of obviousness. M.P.E.P. § 2142 states that

> [t]he examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness.

In particular, Applicants respectfully request that the next Office Action discuss each and every element as set forth by the claims. For example, the Examiner rejected claims 1-8 merely on a

discussion of some of the elements as set forth in claim 1. Claims 2-8 recite elements such as, for example, "a voltage controlled oscillator", "a bandpass filter", "a limiter", "a charge pump" and "a loop filter" as well as other elements (e.g., elements related to the above-recited elements). These elements must be considered and discussed in view of documents cited by the Examiner. Applicants further draw the attention of the Examiner to claims 8-14, which were rejected by merely discussing some of the elements as set forth in claim 8, and to claims 15-21, which were rejected by merely discussing some of the elements as set forth in claim 15.

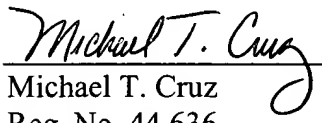
IV. CONCLUSION

In view of at least the foregoing, it is respectfully submitted that the pending claims 1-21 are in condition for allowance. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the below-listed telephone number.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: December 1, 2003

Respectfully submitted,



Michael T. Cruz
Reg. No. 44,636

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8084
Facsimile: (312) 775-8100

DESIGN

Design A Low-Noise Synthesizer Using YRO Technology

This article describes the advantages of the YIG replacement oscillator, and offers a design for a low-noise, fast-switching YRO synthesizer.

ELIOT FENTON AND ANDY GODDARD
APA Wireless Technologies, 4050 N.E. 5th Ave., Fort Lauderdale, FL 33334; (954) 563-8833, FAX: (954) 563-7127, e-mail: efenton@apawireless.com, asgoddard@apawireless.com

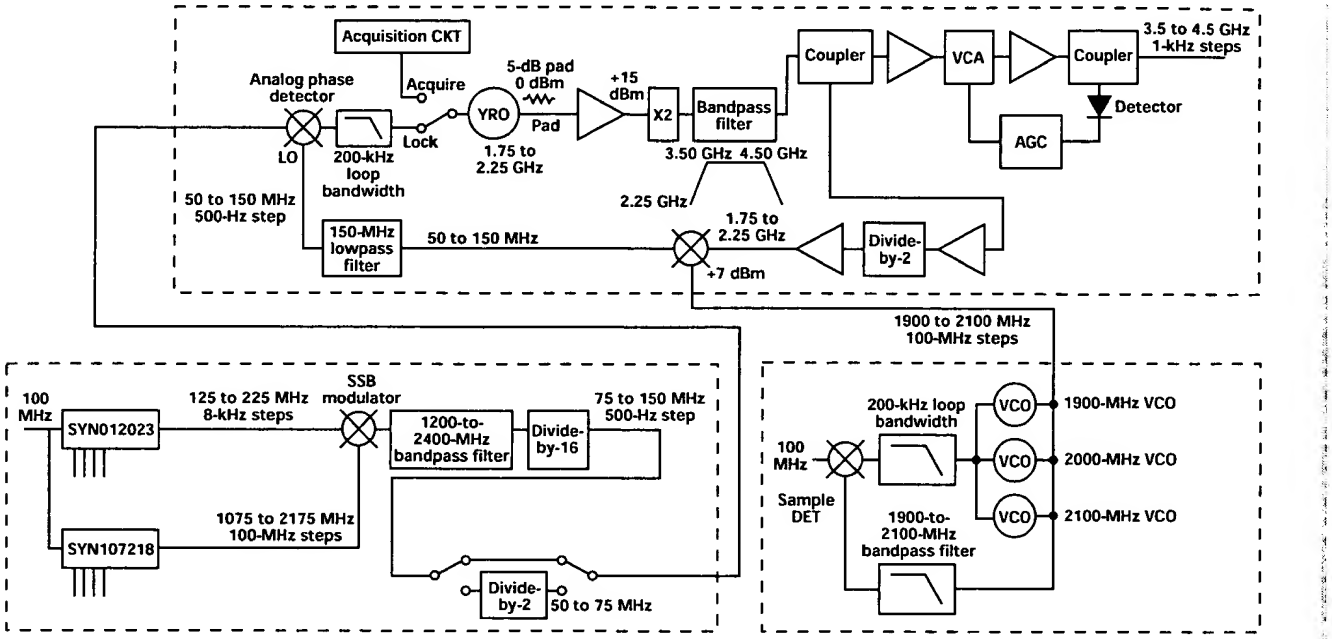
Yttrium-iron-garnet (YIG)-based oscillators are renowned for their ability to generate clean sine waves at very high frequencies, but they are not known for their frequency agility. Nor are they immune to vibrational effects such as microphonics, phase hits, and frequency-modulation (FM) effects. This article describes a novel device called a YIG-replacement oscillator (YRO™), which can serve as a direct substitute for YIGs and dielectric-resonator oscillators (DROs) in applications such as frequency synthesizers, upconverters, downconverters, phase-locked oscillators, microwave communications, test equipment, radar, local multipoint-distribution systems (LMDS), and multichannel multipoint-distribution systems (MMDS). This article describes voltage-controlled oscillators (VCOs), DROs, and YIGs, and points out the advantages that YROs have over these devices. It also describes the design of a fast-switching, low-noise, 3.5-to-4.5-GHz synthesizer that makes use of a YRO.

Traditionally, digital-radio and test-equipment manufacturers used one of two types of oscillators for their products: DROs or YIGs. Mechanically adjustable DROs are used for fixed-frequency applications. Although effective, these components do not have the frequency agility needed for radio manufacturers who build and test their own products. Initially developed for military applications in the 1960s, DROs have a legacy of good performance, albeit with the associated manufacturing difficulties for repeatable performance in high volume at low cost.

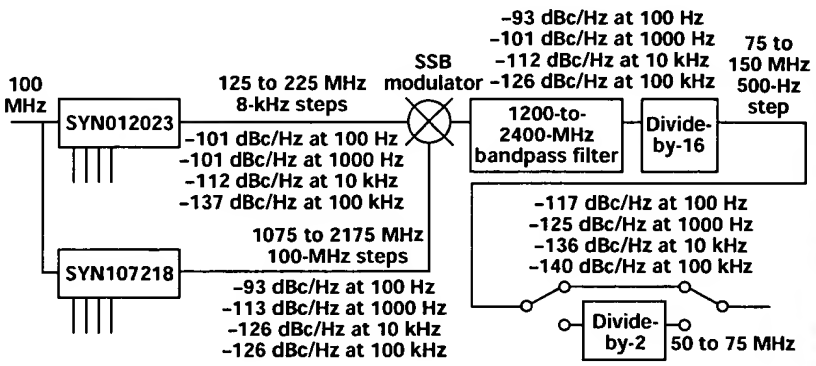
DRO-based radios have limited utility in the LMDS market due to their fixed-frequency nature. To be useful in LMDS applications, they must be combined with additional frequency-agile sources such as VCOs. However, combining DROs and VCOs increases the cost beyond LMDS price points and performance. The fixed-frequency nature of the DRO also precludes their widespread use or adoption in the test-and-measurement market.

To solve the frequency-agility issue, radio manufacturers that serve the point-to-point and point-to-multipoint markets would prefer to use a synthesized application that could emulate the good phase-noise performance of a DRO, yet eliminate the crude DRO-VCO combinations and deliver much higher transmission speeds.

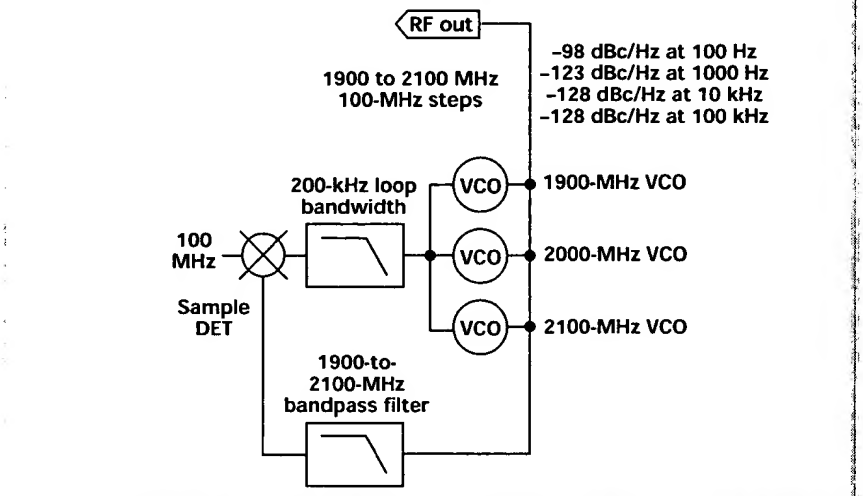
One major technological challenge to increase data rates and improve modulation schemes for digital-radio manufacturers is synthesizing the high-frequency "carrier" wave. To achieve that



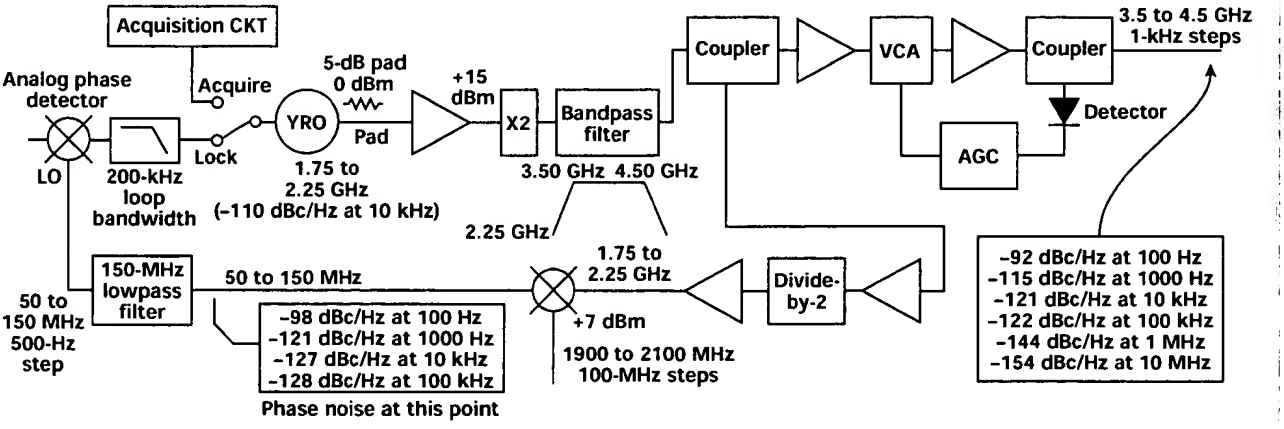
1. The three loops that comprise the synthesizer are illustrated above.



2. This diagram shows the synthesizer's reference loop.



3. The synthesizer's fixed loop is shown here.



4. The synthesizer's main loop can be seen here.

objective, LMDS manufacturers have turned to YIG oscillators. These "analog" devices are capable of generating very-high, very-clean microwave signals that are critical to data transmission. However, YIGs incorporate a rare-earth material that can be difficult to obtain, and the devices must be properly configured in a machined metal housing to be effective.

YIG-based technology has been in use for many years, but it has several inherent weaknesses. For example, YIGs are very expensive to manufacture because they require a substantial amount of manual labor and are prone to manufacturing defects. Also, YIGs can be tuned to different frequencies, but only very slowly.

Unlike conventional VCOs, a YIG-based oscillator's quality-factor (Q) performance increases with frequency, particularly at millimeter-wave frequencies. YIG-based synthesizers provide a superior noise profile, and tuning bandwidths are more than twice that of standard VCO designs. However, YIGs require a significant amount of power, which generates excessive heat that may harm the other electronic components in the transceiver. YIGs also require an environment that is free from vibration and electromagnetic interference (EMI).

In outdoor settings such as a rooftop,

YIGs are prone to wind, vibration, rain, and lightning, all of which have a detrimental effect. For example, YIGs in LMDS systems hanging from rooftops are subject to phase hits, a severe problem affecting the radio's bit-error rate (BER). Interruptions in the carrier signal stemming from a YIG's vibration sensitivity slows and then drops data transmission. This does not bode well for the LMDS system manufacturers in meeting the industry's five-nines (99.999 percent on-signal disruption) standard for reliability. And when a YIG-based synthesizer is destabilized, it is slow to react and re-establish phase lock. This slow reaction contributes to lost transmission bits, increasing BER.

In outdoor settings such as a rooftop, YIGs are prone to wind, vibration, rain, and lightning, all of which have a detrimental effect.

In contrast, YROs have several distinct advantages over YIG technology. First, YROs are silicon (Si)-based devices that can be inexpensively manufactured to very high standards with high repeatability. Second, YROs can change frequencies very rapidly—orders of magnitude faster than a YIG—providing them with a broader range of applications. Third, since YROs oscillate without the need for expensive housing or cumbersome electronics, they are not prone to many of the physical limitations of YIG technology, such as wind, vibration, rain, and EMI.

YROs are fundamental-mode devices that combine the size, ease, and speed of tuning that is associated with a VCO and the phase-noise characteristics of a DRO. Depending on frequency and bandwidth, phase noise can vary from −110 to −120 dBc/Hz at 10-kHz offset.

The following discussion provides a sample design for a 3.5-to-4.5-GHz

synthesizer that offers a step size of 1 kHz and spurious response of −80 dBc.

Design Methodology

When designing low-noise, fast-switching synthesizers, the designer must often assess conflicting requirements to create a balanced product. Covering a gigahertz of bandwidth becomes a challenging proposition if the goal is fast switching, particularly if the frequencies covered are in the 5-GHz spectrum. By adhering to a few simple rules, the design process becomes much easier:

1. Design in excess margin. Start with 10 dB better phase noise than what is required. This will provide the necessary cushion as the design moves forward.

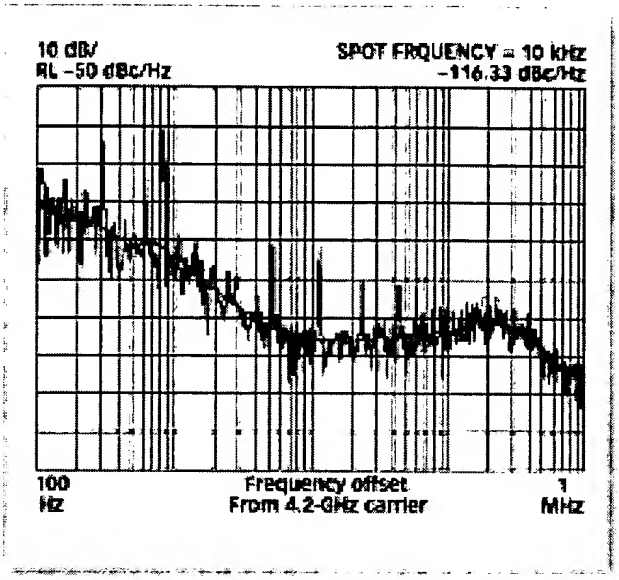
2. Map out an appropriate architecture. This has the largest effect on the design by far, as different architectures accomplish very different roles. Additionally, be sure to analyze the frequency plan for the mixer and other spurious sources.

3. Use local voltage regulation for all VCOs. A clean power supply is crucial for a VCO to operate within its specifications. VCOs in reality have three tuning ports: RF_{out}, which is subject to load pull (pulling), V_{cc}, which is subject to noise modulation (pushing), and, of course, the main tune port. Referring to basic FM modulation theory, noise on the V_{cc} port appears as narrowband FM of the carrier according to the following relationship:

$$L(fm) = 20 \log [KvVnrms \sqrt{2}/(2 fm)]$$

For example, assume that a VCO with a 1-MHz pushing specification (a common value) and a phase noise of −100 dBc/Hz at 10-kHz offset has 1-μVRMS noise on the V_{cc} line. At first glance, this does not appear as excessive noise, but the resulting phase noise at 10 kHz offset will now be degraded to −83 dBc/Hz—which is a significant amount. Additional bypassing would be required to reduce the noise to acceptable levels.

Referring to **Fig. 1**, the synthesizer contains three loops: a reference loop covering 50 to 150 MHz in 500-Hz steps, a fixed loop covering 1900 to 2100 MHz in 100-MHz steps, and a main loop that uses the other two loops in a mixing/doubling architecture. This architecture minimizes phase noise and spurious response by maintaining a low division ratio.



5. This HP 8563E Analyzer plot shows the synthesizer's phase noise.

The reference loop **(Fig. 2)** provides a low-noise reference that steps in small increments and is essentially free of spurious response. It may be tempting to use a direct-digital-synthesizer (DDS)-based scheme. But for spurious-free performance, a DDS requires extensive filtering and is limited in spurious-free bandwidth due to its sampling-based structure. An alternative approach would be a "mix-and-divide scheme," where successive stages are mixed with fixed carriers and divided down to improve phase noise and spurious response. This is often referred to as "direct analog synthesis."

In the reference loop, a 1000-to-1800-MHz, fractionally based synthesizer is divided down by eight, yielding a 125-to-225-MHz, low-noise source that steps in 8-kHz increments. This is mixed with a 1075-to-2175-MHz synthesizer that steps in 100-MHz steps, yielding a 1200-to-2400-MHz signal that steps in 80-kHz increments. An analysis of this mixing scheme does not show any spurs of consequence (<-65 dBc) within ± 5 MHz from the desired carrier, although there are numerous low- and high-order spurs farther out. The higher-order spurs are reduced by using appropriate lowpass filtering, and the resultant signal is then divided down by a factor of 16 (or 32), yielding a 50-to-150-MHz, low-noise signal that steps in 500-Hz increments, with less than -85-dBc spurious response.

This loop **(Fig. 3)** uses a sampling phase detector (SPD) and three VCOs to generate 1900 to 2100 MHz. A sampling phase detector consists of a step-recovery diode (SRD) capacitively coupled to two back-to-back Schottky diodes, which act as a mixer. The SRD, when properly driven by a 100-MHz source, generates harmonics through several gigahertz. These harmonics mix with the desired carrier (at the Schottky diodes) yielding an intermediate frequency (IF) that is suitable for phase lock. For example, to phase lock the 2100-MHz VCO, the SRD is driven by a 100-MHz signal and generates a 100-MHz comb, which includes a 2100-MHz signal. This 2100-MHz signal is mixed with the VCO's carrier, and the resultant IF signal controls an active loop filter which, in turn, adjusts the VCO's tuning voltage to compensate for phase and frequency fluctuations.

The advantage of using an SPD as opposed to a digital phase detector is the SPD's superior phase-noise characteristics, and the improvement in overall loop gain. A typical SPD-based loop has a noise floor of -155 dBc/Hz at the diodes, and a loop-division ratio of one. This would yield a theoretical noise floor of -127.4 dBc/Hz at 2.1 GHz ($[20\log(2400/100)]-155$). Compared

to a digital phase detector, this is a 27-dB improvement. The disadvantage of an SPD is the requirement for pre-steering the VCO to aid in acquisition. Unlike a digital phase detector that will lock and acquire more than a ±2-Π range, the analog phase detector has limited acquisition capability and requires the assistance of an external circuit.

Main Loop

The goal of the main loop **(Fig. 4)** is to generate a spurious-free 3.5-to-4.5-GHz signal. As with the fixed loop, an analog phase detector must be used to satisfy the phase-noise requirements. This, however, brings additional problems in signal acquisition. APA Wireless has developed proprietary patent-pending techniques that fully leverage the superior phase-noise characteristics of analog phase detectors with the wide-tuning and acquisition capabilities of digital phase detectors. Referring to the main loop section shown in Fig. 1, the acquisition circuitry will set the YRO to the exact desired frequency in less than 10 µs, and does so in parallel with the other loops, regardless of step size.

Circuit Description

In order to satisfy the phase-noise requirements at offsets that are far from the carrier, a signal source (VCO or YIG) that can cover wide bandwidths, yet maintain good phase noise must be used. Although a YIG would satisfy this requirement, it lacks the frequency agility needed for sub-100-µs switching and requires additional circuitry for phase-lock operation. APA developed its line of YROs to address this issue, with phase noise rivaling YIG solutions but without the driver complexity.

Referring to the block diagram that is shown in Fig. 3, a 1.75-to-2.25-GHz YRO drives a doubler to achieve a 3.5-to-4.5-GHz output. Although a 3.4-to-4.5-GHz YRO could have been used, the doubled approach offers the following advantages:

- The divider provides isolation between the fixed-frequency loop and the main output. Without the divider, frequencies close to the desired final frequency would have to be mixed into the main loop. These frequencies would appear at the main output, and would be virtually impossible to filter or remove.
- The divider eases the fixed loop-frequency requirement. Half as many frequencies are needed.

YROs are fundamental-mode devices that combine the size, ease, and speed of tuning associated with a VCO and the phase-noise characteristics of a DRO.

The doubled output is then divided by two, and drives a series of isolation amplifiers, which drive a mixer whose RF port is driven by the fixed loop. The resultant IF signal drives the local-oscillator (LO) port of an analog phase detector whose RF port is driven by the reference loop. In this way, the reference loop provides fine frequency control over 100-MHz bandwidths, with the fixed loop incrementing the coarse frequency in 100-MHz steps.

Since the phase noise of the YRO is −130 dBc/Hz at a 100-kHz offset and the noise floor of the fixed loop is −128 dBc/Hz, the loop-bandwidth crossover point for phase noise is set at the 100-kHz point. Of course, since the fixed loop sets the noise floor for this architecture, improvements in this area will yield better phase noise, up until the limit that is set by the reference loop (−140 dBc/Hz at 100-kHz offset). The doubled output is filtered in order to remove subharmonics, then drives an automatic-gain-controlled (AGC) final amplifier.

Figure 5 is a phase-noise plot (using an HP 8563E spectrum analyzer) of the output of the previously described synthesizer at 4.2 GHz—clearly at the limits of the analyzer. MRF